In the Claims:

Please cancel Claims 1-13 and amend Claim 18 as indicated below. The status of all claims is as follows:

1-13. (Cancelled)

14. (Original) A thin film transistor substrate comprising:

a substrate;

a first transistor structure having a first semiconductor layer formed on said substrate, a first gate insulating film and a first gate electrode, wherein a channel region of said first semiconductor layer under said first gate electrode is intentionally doped with only p-type impurities, said first semiconductor layer includes n-type LDD regions outside the channel region and high impurity concentration n-type source/drain regions outside the n-type LDD regions, and said first gate electrode is made of a lamination of a first metal layer and a second metal layer;

a second transistor structure having a second semiconductor layer formed on said substrate, a second gate insulating film and a second gate electrode, wherein a channel region of said second semiconductor layer under said second gate electrode is intentionally doped with only p-type impurities, said second semiconductor layer includes high impurity

concentration n-type source/drain regions outside the channel region, and said second gate electrode is made of a lamination of said first metal layer and said second metal layer; and

a third transistor structure having a third semiconductor layer formed on said substrate, a third gate insulating film and a third gate electrode, wherein a channel region of said third semiconductor layer under said third gate electrode is intentionally doped with p-type impurities and n-type impurities, said third semiconductor layer includes high impurity concentration p-type source/drain regions outside the channel region, and said third gate electrode is made of said second metal layer.

15. (Original) The thin film transistor substrate according to claim 14, wherein said second semiconductor layer has n-type LDD regions outside the channel region, and the high impurity concentration n-type source/drain regions outside the n-type LDD regions.

16. (Original) The thin film transistor substrate according to claim 14, wherein said first and second metal layers have different etching characteristics.

17. (Original) The thin film transistor substrate according to claim 16, wherein said first metal layer is a refractory metal layer and said second metal layer is an aluminum alloy layer.

18. (Currently Amended) A thin film transistor substrate comprising:

a substrate;

a first transistor structure having a first semiconductor layer formed on said substrate, a first gate insulating film and a first gate electrode, wherein a channel region of said first semiconductor layer under said first gate electrode is intentionally doped with only p-type impurities, said first semiconductor layer includes n-type LDD regions outside the channel region and high impurity concentration n-type source/drain regions outside the n-type LDD regions, and said first gate electrode is made of a second metal layer;

a second transistor structure having a second semiconductor layer formed on said substrate, a second gate insulating film and a second gate electrode, wherein a channel region of said second semiconductor layer under said second gate electrode is intentionally doped with p-type impurities at the first impurity concentration, said second semiconductor layer includes high impurity concentration n-type source/drain regions outside the channel region, and said second gate electrode is made of said second metal layer; and

a third transistor structure having a third semiconductor layer formed on said substrate, a third gate insulating film and a third gate electrode, wherein a channel region of said third semiconductor layer under said third gate electrode is intentionally doped with p-type impurities at a second impurity concentration lower than the first impurity concentration, said third semiconductor layer includes high impurity concentration p-type source/drain

regions outside the channel region, and said third gate electrode is made of a ~~first~~ second metal layer that is different from said first metal layer.

19. (Original) The thin film transistor substrate according to claim 18, wherein said second semiconductor layer has n-type LDD regions outside the channel region, and the high impurity concentration n-type source/drain regions outside the n-type LDD regions.

20. (Original) The thin film transistor substrate according to claim 18, wherein said first metal layer has etching characteristics different from those of said second metal layer.

21. (Original) The thin film transistor substrate according to claims 20, wherein said first metal layer is a refractory metal layer and said second metal layer is an aluminum alloy layer.